8085 Interrupt

INTRODUCTION

what is Interrupt?

Interrupt is a mechanism by which an I/O or an instruction can suspend the normal execution of processor and get itself serviced. Generally, a particular task is assigned to that interrupt signal. In the microprocessor based system the interrupts are used for data transfer between the peripheral devices and the microprocessor.

- After receiving an interrupt signal from the peripheral, the microprocessor executes current instruction completely.

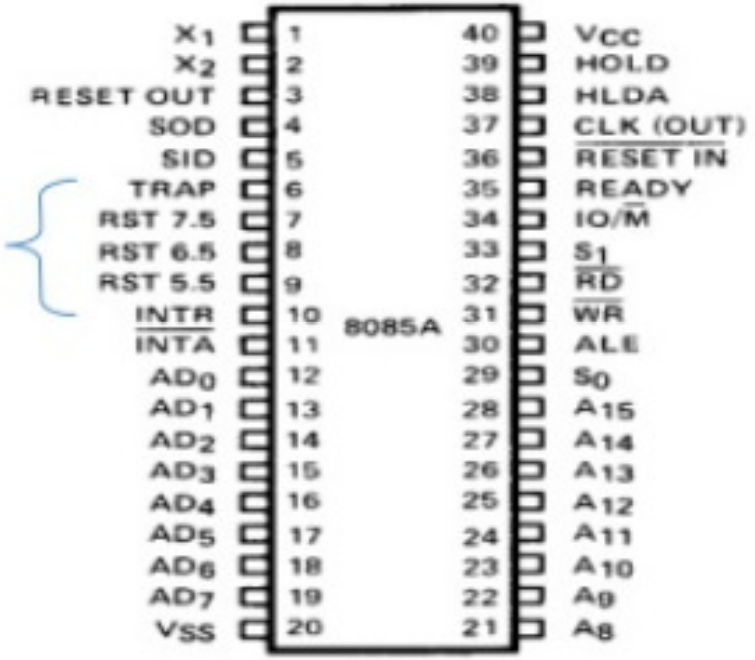
- Store the contents of program counter i.e. return address on the stack and then executes interrupts service (ISR) to provide service to the interrupting device.

- After servicing the device, the microprocessor transfer program control back to the program where interrupt occurs by reloading the content of program counter which has been stored on the stack when an interrupt occurs.

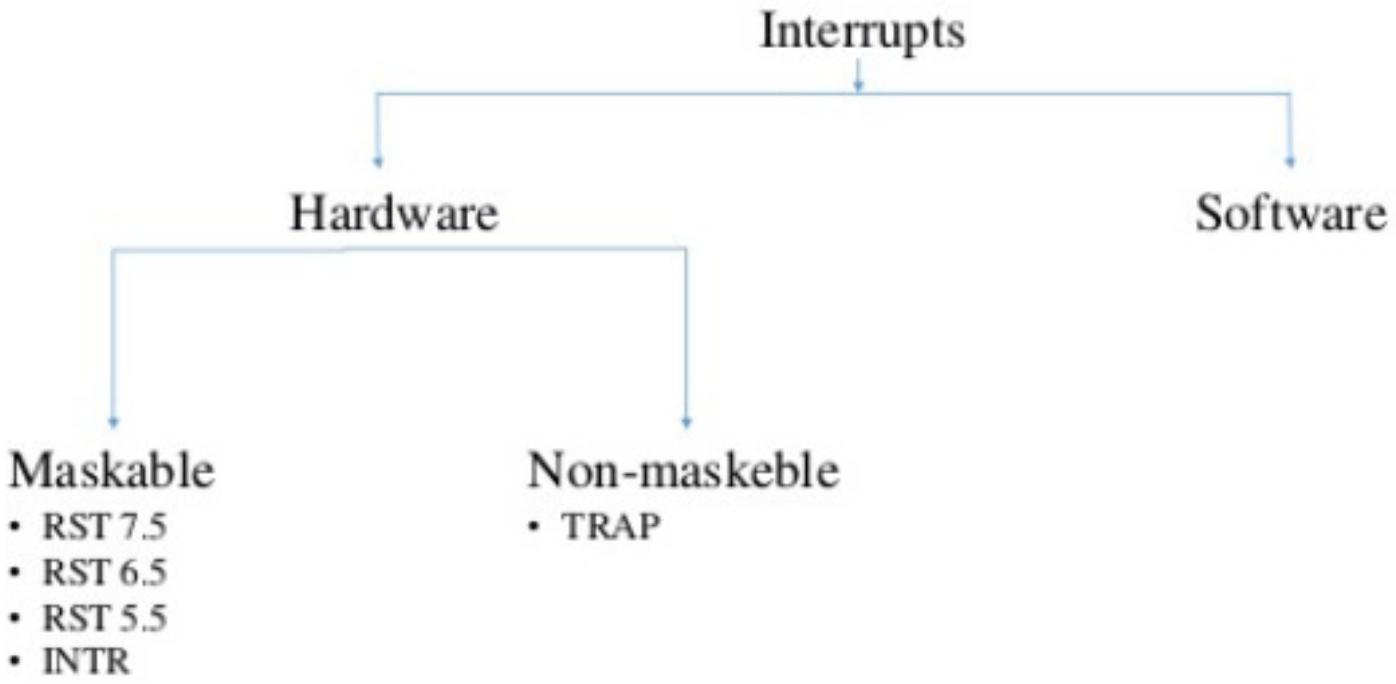
Interrupts pin on IC :-

There are 5 interrupt inputs:

1) TRAP (non-maskable)
2) RST7.5
3) RST6.5
4) RST5.5
5) INTR



CLASSIFICATION OF INTERRUPTS



HARDWARE INTERRUPTS

Nonmaskable interrupt

The MPU is interrupted when a logic signal is applied to this type of input.

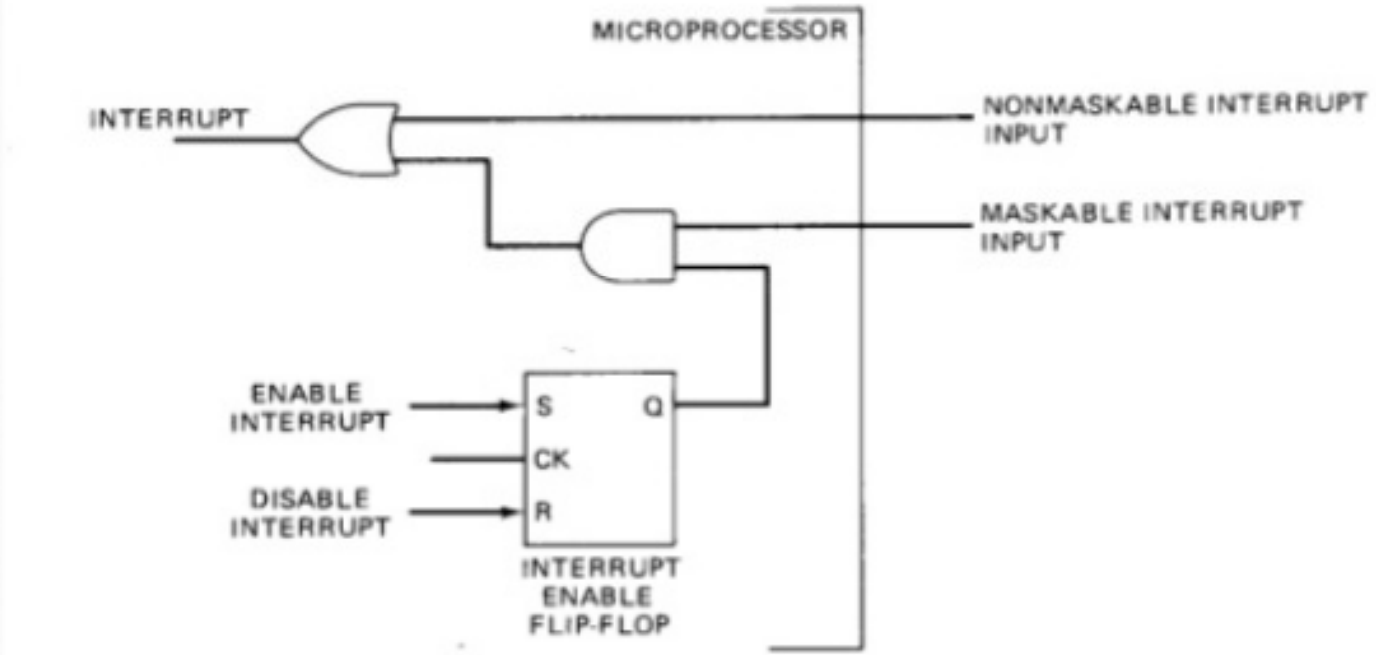
Maskable interrupt

The MPU is interrupted ONLY if that particular input is enabled.

It is enabled or disabled under program control.

If disabled, an interrupt signal is ignored by the MPU.

Maskable & Nonmaskable INT



- **Hardware and Software Interrupts –**

When microprocessors receive interrupt signals through pins (hardware) of microprocessor, they are known as *Hardware Interrupts*. There are 5 Hardware Interrupts in 8085 microprocessor. They are – *INTR, RST 7.5, RST 6.5, RST 5.5, TRAP*.

Software Interrupts are those which are inserted in between the program which means these are mnemonics of microprocessor. There are 8 software interrupts in 8085 microprocessor. They are – *RST 0, RST 1, RST 2, RST 3, RST 4, RST 5, RST 6, RST 7*.

- Interrupts can be classified into two types:
  - Maskable Interrupts (Can be delayed or Rejected)
  - Non-Maskable Interrupts (Can not be delayed or Rejected)
- Interrupts can also be classified into:
  - Vectored (the address of the service routine is hard-wired)
  - Non-vectored (the address of the service routine needs to be supplied externally by the device)

- Nonmaskable interrupt input
  - The MPU is interrupted when a logic signal is applied to this type of input.
- Maskable interrupt input
  - The MPU is interrupted ONLY if that particular input is enabled.
  - It is enabled or disabled under program control.
    - If disabled, an interrupt signal is ignored by the MPU.

- **Vectored and Non-Vectored Interrupts –**

Vectored Interrupts are those which have fixed vector address (starting address of sub-routine) and after executing these, program control is transferred to that address.
Non-Vectored Interrupts (Scalar Interrupt) are those in which vector address is not predefined. The interrupting device gives the address of sub-routine for these interrupts. *INTR* is the only non-vectored interrupt in 8085 microprocessor.

- **Maskable and Non-Maskable Interrupts –**

Maskable Interrupts are those which can be disabled or ignored by the microprocessor. These interrupts are either edge-triggered or level-triggered, so they can be disabled. *INTR, RST 7.5, RST 6.5, RST 5.5* are maskable interrupts in 8085 microprocessor.

Non-Maskable Interrupts are those which cannot be disabled or ignored by microprocessor. *TRAP* is a non-maskable interrupt. It consists of both level as well as edge triggering and is used in critical power failure conditions.

Response to Interrupt

- Responding to an interrupt may be immediate or delayed depending on whether the interrupt is maskable or non-maskable and whether interrupts are being masked or not.
- MP completes its current machine cycle.
- There are two ways of redirecting the execution to the ISR depending on whether the interrupt is vectored or non-vectored.
  - Vectored: The address of the subroutine is already known to the Microprocessor
  - Non Vectored: The device will have to supply the address of the subroutine to the Microprocessor

8085 INTERRUPTS

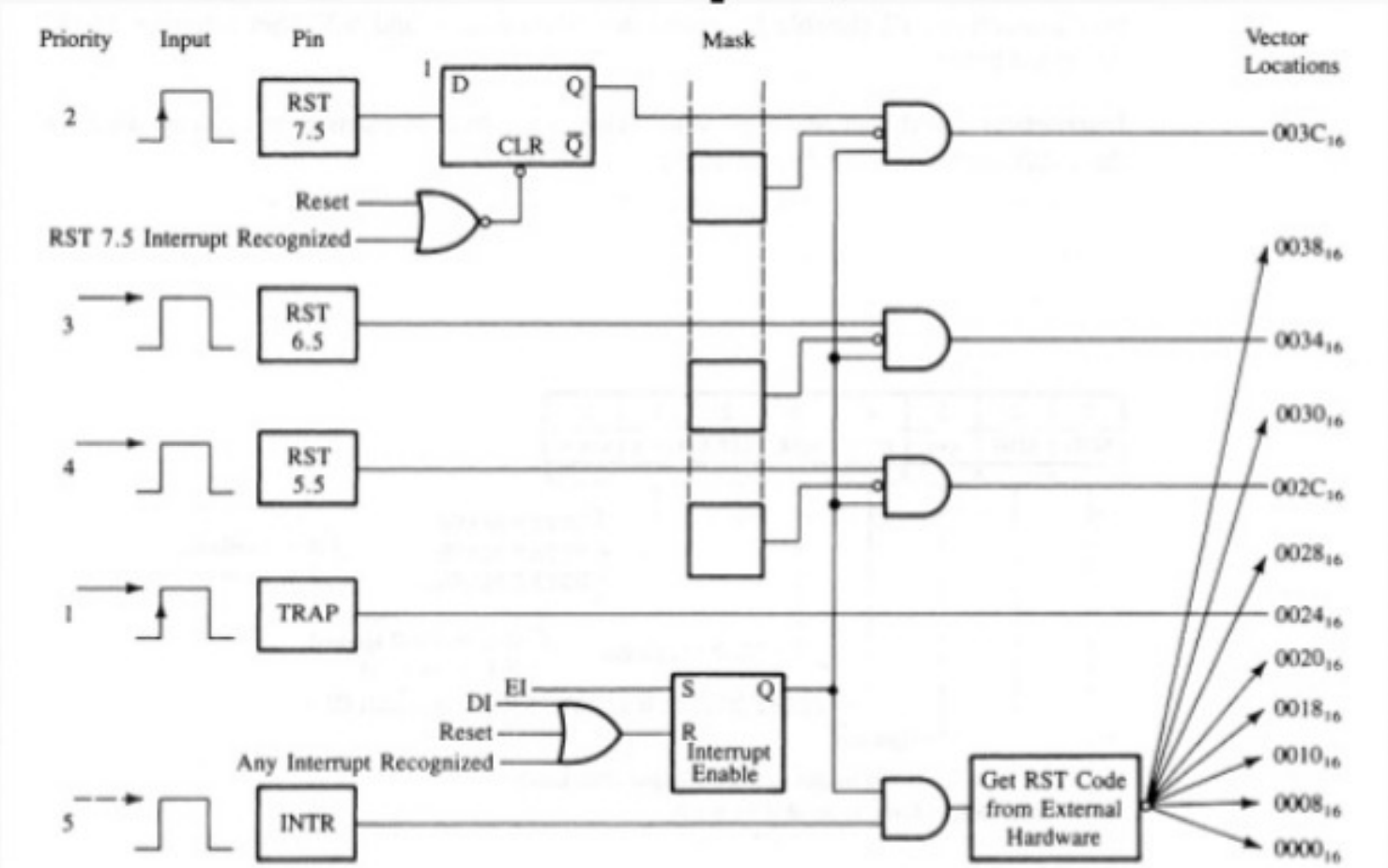
- The 'EI' instruction is a one byte instruction and is used to Enable the maskable interrupts.
- The 'DI' instruction is a one byte instruction and is used to Disable the maskable interrupts.
- The 8085 has a single Non-Maskable
- The 8085 has 5 interrupt inputs.
  - The INTR input.
    - The INTR input is the only non-vectored interrupt.
    - INTR is maskable using the EI/DI instruction pair.
  - RST 5.5, RST 6.5, RST 7.5 are all automatically vectored.
    - RST 5.5, RST 6.5, and RST 7.5 are all maskable.

8085 INTERRUPTS

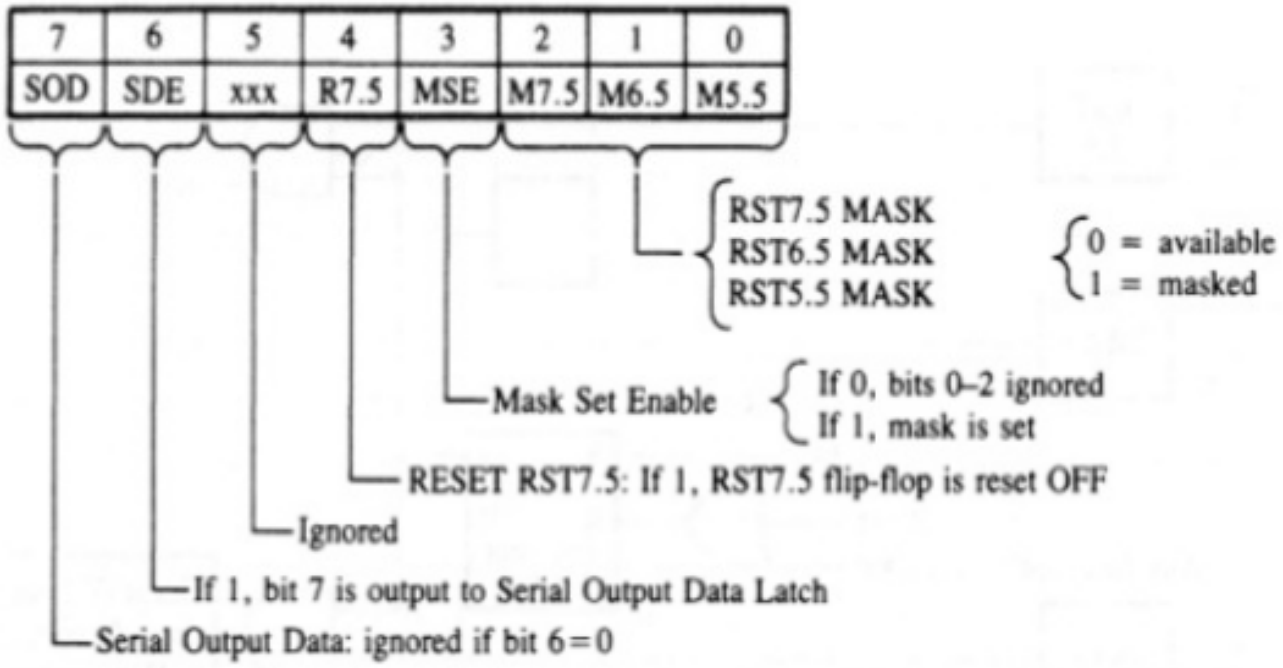
- TRAP is the only non-maskable interrupt in the 8085
  - TRAP is also automatically vectored

Interrupt Name	Maskable	Vectored
INTR	Yes	No
RST 5.5	Yes	Yes
RST 6.5	Yes	Yes
RST 7.5	Yes	Yes
TRAP	No	Yes

Vectored Interrupts



SIM Instruction



Assignment

- What is RIM?
- Draw the Accumulator bit pattern for RIM instruction.
- Describe the RIM instruction using an example.